CLAIMS

1. An image sensor array comprising:

a plurality of pixels arranged in rows and columns, each pixel including a contact pad and pixel circuitry connected to the contact pad;

a passivation layer defining a plurality of trenches, each trench being surrounded by passivation walls having upper edges, wherein the contact pad of each pixel is located in an associated trench such that an upper surface of the contact pad is located below the upper edges of the passivation walls;

a sensor layer formed over the passivation layer and having lower portions extending into the trenches, wherein each lower portion of the sensor layer abuts the upper surface of an associated pixel contact pad.

2. The image sensor array according to Claim 1, wherein the sensor layer is an amorphous silicon (a-Si:H) layer further comprising:

an upper region that is doped with a p-type dopant; and

an undoped central region that is located between the upper region and the lower portions,

wherein the lower portions of the a-Si:H layer that are doped with an n-type dopant, and

wherein the passivation walls extend into the central, relatively undoped region of the a-Si layer.

3. The image sensor array according to Claim 1, further comprising a conductor formed below each of the passivation walls, wherein the conductor is connected to a

low voltage source such that the conductor generates a field that impedes the flow of electrons from a metal contact pad of a first pixel to a metal contact pad of a second pixel via the passivation wall.

4. The image sensor array according to Claim 3, wherein portions of selected conductors extend under the contact pad of associated pixels such that a capacitor is formed by each portion and the contact pad of the associated pixel.

5. The image sensor array according to Claim 1,

wherein the sensor layer is an amorphous silicon (a-Si:H) layer further comprising an upper region that is doped with a p-type dopant, and a central region that is located between the upper region and the lower portions, and

wherein the central region and the lower portions of the a-Si:H layer are undoped.

6. The image sensor array according to Claim 1, wherein side surfaces of the the passivation walls are sloped such that the lower portion of the a-Si:H layer forms an angle in the range of 45° and 60° relative to the upper surface of the contact pad.

7. The image sensor array according to Claim 6, further comprising a conductor formed below each of the passivation walls, wherein the metal structure is connected to a low voltage source such that the metal structure generates a field that impedes the flow of electrons from a

metal contact pad of a first pixel to a metal contact pad of a second pixel via the passivation wall.

8. The image sensor array according to Claim 6, wherein the passivation walls are formed from a material selected from the group consisting of SiO_2, SiON, and benzocyclobutene (BCB).

9. A image sensor array comprising:

a plurality of pixels including a first pixel having a first contact pad and a second pixel having a second contact pad that is separated from the first contact pad by an elongated interface region;

a continuous sensor layer formed over the plurality of pixels and having lower portions contacting the first and second contact pads, respectively; and

a plurality of conductors including a first conductor extending under the interface region separating the first and second contact pads,

wherein the plurality of conductors are connected to a low voltage source such that the first conductor generates a field that impedes the flow of electrons across the interface region from the first contact pad of the first pixel to the second contact pad of the second pixel.

10. The image sensor array according to Claim 9, wherein the first conductor further comprises a portion extending under the first contact pad such that a capacitor is formed by the portion and the first contact pad.

11. The image sensor array according to Claim 9, further comprising a passivation layer including portions provided in the interface region separating the first and second contact pads.

12. The image sensor according to Claim 11,

wherein the passivation layer defines a plurality of trenches and the portions of the passivation layer comprise passivation walls surrounding the trenches, each of the passivation walls having upper edges, and

wherein the first contact pad is located in a first trench and the second contact pad is located in a second trench adjacent to the first trench such that a first passivation wall is located between the first contact pad and the second contact pad, and such that the upper surfaces of the first and second contact pads are located below the upper edge of the first passivation wall.

13. The image sensor array according to Claim 12, wherein the passivation walls are formed from a material selected from the group consisting of SiO_2, SiON, and benzocyclobutene (BCB).

14. The image sensor array according to Claim 12, wherein the passivation walls are sloped such that the lower portions of the central region of the continuous sensor layer define an angle in the range of 45° and 60° relative to the upper surface of the contact pad.

15. The image sensor array according to Claim 9, wherein the continuous sensor layer is an amorphous silicon (a-Si:H) layer further comprising:

an upper region that is doped with a p-type dopant; and

an undoped central region that is located between the upper region and the lower portions,

wherein the lower portions of the a-Si:H layer that are doped with an n-type dopant, and

wherein the passivation walls extend into the central, relatively undoped region of the a-Si:H layer.

16. The image sensor array according to Claim 9,

wherein the continuous sensor layer is an amorphous silicon (a-Si:H) layer further comprising an upper region that is doped with a p-type dopant, and a central region that is located between the upper region and the lower portions, and

wherein the central region and the lower portions of the a-Si:H layer are undoped.

17. A image sensor array comprising:

a plurality of pixels arranged in rows and columns, each pixel including a contact pad and pixel circuitry connected to the contact pad; and

a continuous amorphous silicon layer formed over the plurality of pixels, the amorphous silicon layer including a continuous doped region and a continuous intrinsic region located under the doped region and contacting an upper surface of the contact pad of each of the plurality of pixels.

18. The image sensor array according to Claim 17,

wherein the plurality of pixels include a first pixel having a first contact pad and a second pixel having a second contact pad separated from the first contact pad by an interface region, and

wherein the sensor array further comprises a passivation layer including portions provided in the interface region separating the first and second contact pads.

19. The image sensor according to Claim 18,

wherein the passivation layer defines a plurality of trenches and the portions of the passivation layer comprise passivation walls surrounding the trenches, each of the passivation walls having upper edges, and

wherein the first contact pad is located in a first trench and the second contact pad is located in a second trench adjacent to the first trench such that a first passivation wall is located between the first contact pad and the second contact pad, and such that the upper surfaces of the first and second contact pads are located below the upper edge of the first passivation wall.

20. The image sensor according to Claim 18, further comprising a plurality of conductors including a first conductor extending under the interface region separating the first and second contact pads,

wherein the plurality of conductors are connected to a low voltage source such that the first conductor generates a field that impedes the flow of electrons across the

interface region from the first contact pad of the first pixel to the second contact pad of the second pixel.